IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/649,450	Confirmation No.: 5775
Applicant	:	Michael Doogue, et al.	
Filed	:	August 26, 2003	
T.C./A.U.	:	2831	
Examiner	:	Hung V. Ngo	
Docket No.	:	ALLEG-039PUS	
Customer No.	:	022494	

SUPPLEMENTAL APPEAL BRIEF UNDER 37 C.F.R. 41.37

MS Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Supplemental Appeal Brief replaces an Appeal Brief originally filed on November 5, 2008, and also replaces amendments thereto filed in Responses to Notifications of Non-Compliant Appeal Briefs filed on April 27, 2009 and July 17, 2009. This Supplemental Appeal Brief also makes current an Internet link at the bottom of page 6. Subject matter at the new link is substantially the same as subject matter at the old and no longer current link.

In response to the final Office Action dated October 8, 2008, which finally rejected Claims 1, 4-11, 13-18, 29, 30, 32, 33, 36-38, 40, and 41, and which objected to Claims 12 and 31 in the above-identified application, please consider the arguments set forth below.

Claims currently in the application are provided as an attachment hereto.

Table of Authorities

The following authorities are referred to herein:

1) In re Ratti, 270 F.2d 810, 123 USPQ 349 (C.C.P.A. 1959)

2) Federal Register, Volume 72, No. 195, dated October 10, 2007, page 57528, Part III of the section entitled "Examination Guidelines for Determining Obviousness under 35 U.S.C. 103 in View of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.*"

(i) Real Party in Interest

Allegro Microsystems, Inc. is the real party in interest by way of an assignment executed on August 26, 2003 by inventors Michael Doogue, Richard Dickinson, and Jay Gagnon, the previous parties in interest, which was recorded on reel 014246, frames 0286-0289, on January 9, 2004.

(ii) Related Appeals and Interferences

None

(iii) Status of the Claims

Claims 1, 4-11, 13-18, 29, 30, 32, 33, 36-38, 40, and 41 remain rejected. Claims 1 and 29 are independent claims. Claims 12 and 31 are objected to but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1, 4-11, 12, 13-18, 29, 30, 31, 32, 33, 36-38, 40, and 41 are appealed. Claims 2, 3, 19-28, 34, 35, and 39 were previously canceled.

Claims 11, 4-11, 13-18, 29, 30, 32, 33, 36-38, 40, and 41 stand rejected on bases set forth in the Final Office Action dated October 8, 2008. In particular:

1) Claims 1, 4-7, 13, 14, 17, 18, 29, 30, 32, 33, 40 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida (EP Patent number 0867725);

2) Claim 8 is rejected under 35 U.S.C. §103(a) as being obvious over Ishida in view of Yangawa et al. (U.S. Patent Publication number 2001/0028115);

3) Claims 9, 36, and 37 are rejected under 35 U.S.C. §103(a) as being obvious over Ishida in view of Williams (U.S. Patent Publication number 2005/0230843); and

4) Claims 10, 11, 15, 16, and 38 are rejected under 35 U.S.C. §103(a) as being obvious over Ishida in view of Mayer et al. (U.S. Patent Publication number 2002/0179987).

In addition, as described above, Claims 12 and 31 stand objected to as set forth in the Final Office Action dated October 8, 2008 but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(iv) Status of Amendments Filed After Final Rejection

No amendments to the claims were filed after the final rejection dated October 8, 2008.

(v) Summary of Claimed Subject Matter

One aspect of the claimed invention (Claim 1) is directed to an integrated circuit having particular characteristics. In particular, the integrated circuit includes a lead frame having a current conductor formed from a coupling of at least two leads of the lead frame. The integrated circuit also includes a substrate on which one or more magnetic field transducers are disposed. The substrate is disposed in a flip-chip arrangement relative to the lead frame so that the one or more magnetic field transducers are particularly close to the current conductor resulting in an increased sensitivity of the integrated circuit to a magnetic field.

The claimed flip-chip arrangement is described throughout the specification, for example, in conjunction with FIG. 1. Applicants submit that it is notoriously well known that a flip-chip arrangement results in a lead frame above a circuit board to which it mounts and a substrate above at least the base plate of the lead frame, wherein an active surface of the substrate is flipped, i.e., disposed downward toward the lead frame. The active surface will be understood to be the surface of the substrate on which electronic components are disposed.

Another aspect of the claimed invention (Claim 29) is directed to an integrated circuit having other particular characteristics. In particular, the integrated circuit includes a lead frame having a current conductor formed from a coupling of at least two leads of the lead frame to form a loop. The integrated circuit also includes a substrate onto which one or more magnetic field transducers are disposed. The one or more magnetic field transducers are disposed proximate to the loop so that they are responsive to a current flowing through the loop.

From claim language (Claim 29) presented below, it will be recognized that the claimed loop is a part of the integrated circuit.

Regarding independent Claim 1, referring to FIG. 1 of the present application, which is described from pages 4-6 of the specification, and using reference designators like those thereupon, independent Claim 1 provides an integrated circuit (10), comprising: a lead frame (12) having a plurality of leads (12a-12h) and having a current conductor portion (14) comprising a coupling of at least two (12a, 1b, 12c, 12d) of the plurality of leads (12a-12h), each one of the leads (12a-12h) having a respective length; a substrate (16) having first (16a) and second (16b) opposing surfaces, the first surface (16a) proximate to the current conductor portion (14) and the second surface (16b) distal from the current conductor portion (14), wherein at least some of the leads (12a-12h) of said lead frame (12) are electrically coupled to said substrate (14); and one or more magnetic field transducers (18) disposed on the first surface (16a) of said substrate (16), wherein said substrate (16) and said lead frame (12) are relatively disposed in a flip-chip arrangement (page 4, lines 16-23) resulting in the current conductor portion (14) being proximate to said one or more magnetic field transducers (18), and further resulting in an increased sensitivity of the integrated circuit (10) to a magnetic field.

As described at page 5, beginning at line 13:

> With this arrangement, the Hall effect element 18 is disposed in close proximity to the current conductor portion 14 and at a predetermined position relative to the conductor portion 14, such that a magnetic field generated by an electrical current passing though the current conductor portion 14, in a direction

> shown by arrows 26, is in a direction substantially aligned with a maximum response axis of the Hall effect element 18. The Hall effect element 18 generates a voltage output proportional to the magnetic field and therefore proportional to the current flowing through the current conductor portion 14. The illustrated Hall effect element 18 has a maximum response axis substantially aligned with a z-axis 34. Because the magnetic field generated in response to the current is circular about the current conductor portion 14, the Hall effect element 18 is disposed just to the side (i.e., slightly offset along a y-axis 32) of the current conductor portion 14, as shown, where the magnetic field is pointed substantially along the z-axis 34. This position results in a greater voltage output from the Hall effect element 18, and therefore improved sensitivity. However, a Hall effect element, or another type of magnetic field sensor, for example a magnetoresistance element, having maximum response axis aligned in another direction, can be disposed at another position relative to the current conductor portion 14, for example, on top of the current conductor portion 14 (in a direction along z-axis 34).

Regarding independent Claim 29, referring again to FIG. 1 of the present application, which is described from pages 4-6 of the specification, and using reference designators like those thereupon, independent Claim 29 provides an integrated circuit (10), comprising a lead frame (12) having a plurality of leads (12a-12h) and having a current conductor portion (14) comprising a coupling of at least two of the plurality of leads (12a, 12b, 12c, 12d), wherein the coupling of at least two of the plurality of leads comprises a loop (14 with 12a-12d), the at least two of the leads (12a-12b, 12c, 12d) and the loop (14 with 12a-12d) forming a continuous electrical path entirely formed of lead frame material; a substrate (16) having first (16a) and second (16b) opposing surfaces, the first surface (16a) proximate to the current conductor portion (14) and the second surface (16b) distal from the current conductor portion (14), wherein at least some of the leads (12a-12h) of said lead frame (12) are electrically coupled to said substrate (16); and one or more magnetic field transducers (18) disposed on the first surface (16a) of said substrate (16) and proximate to the loop (14 with 12a-12d) such that the one or more magnetic field transducers (18) are responsive to a current flowing through the loop (14 with 12a-12d).

(vi) Grounds of Rejections to Be Reviewed On Appeal

Issues presented for appeal include the following:

1) Whether Claims 1, 4-7, 13, 14, 17, 18, 29, 30, 32, 33, 40 and 41 are anticipated by Ishida (EP Patent number 0867725);

2) Whether Claim 8 is obvious over Ishida in view of Yangawa et al. (U.S. Patent Publication number 2001/0028115);

3) Whether Claims 9, 36, and 37 are obvious over Ishida in view of Williams (U.S. Patent Publication number 2005/0230843);

4) Whether Claims 10, 11, 15, 16, and 38 are obvious over Ishida in view of Mayer et al. (U.S. Patent Publication number 2002/0179987); and

5) Whether dependent Claims 12 and 31 are allowable in their present dependent form.

(vii) Argument

A. Claims 1, 4-7, 13, 14, 17, 18, 29, 30, 32, 33, 40 and 41 are not anticipated by Ishida (EP Patent number 0867725)

Applicants submit that independent Claim 1 is patentably distinct over Ishida, since the cited reference neither describes nor suggests "... *a lead frame having a plurality of leads and having a current conductor portion comprising a coupling of at least two of the plurality of leads*...; a substrate... wherein *at least some of the leads of said lead frame are electrically coupled to said substrate*; and one or more magnetic field transducers disposed on the first surface of said substrate, *wherein said substrate and said lead frame are relatively disposed in a flip-chip arrangement resulting in the current conductor portion being proximate to said one or more magnetic field transducers*, and further resulting in an increased sensitivity of the integrated circuit to a magnetic field," as set forth in Claim 1.

The Examiner asserts that the structure 1a of Ishida is a current conductor portion. However, Applicants submit that the structure 1a of Ishida is not part of a lead frame as claimed.

A lead frame is decribed in on-line Wikipedia at http://en.wikipedia.org/wiki/Semiconductor_fabrication :

> Plastic or ceramic packaging involves mounting the die, connecting the die pads to the pins on the package, and sealing the die. Tiny wires are used to connect pads to the pins. In the old days, wires were attached by hand, but now purpose-built machines perform the task. Traditionally, the wires to the chips were gold, leading to a "lead frame" (pronounced "leed frame") of copper, that had been plated with solder, a mixture of tin and lead. Lead is poisonous, so lead-free "lead frames" are now the best practice.

Applicants submit that the term lead frame is notorioulsy well known in the semiconductor industry. The lead frame in integral to the integrated circuit and it is that structure to which electrical contacts are made from a substrate (die). Applicants submit that the term lead frame should be construed in accordance with its ordinary meaning.

Applicants also respectfully direct the Examiner's attention to the language of Claim 1, which recites "at least some of the leads of said lead frame are electrically coupled to said substrate." Thus, the conductor 1 of Ishida cannot be a lead frame as recited in the claims.

Furthermore, as described above, the flip-chip arrangement is described throughout the specification, for example, in conjunction with FIG. 1. Applicants submit that it is notoriously well known that a flip-chip arrangement results in a lead frame above a circuit board to which it mounts and a substrate above at least the base plate of the lead frame, wherein an active surface of the substrate is flipped, i.e., disposed downward toward the lead frame. The active surface will be understood to be the surface of the substrate on which electronic components are disposed.

In contrast, the arrangement of Ishida does not teach a flip-chip at all. Ishida does not describe any arrangement between a substrate and a lead frame.

In view of the above, Applicants submit that Claim 1 is patentably distinct over Ishida.

Claims 4-7, 13, 14, 17, 18, and 40 depend from and thus include the limitations of Claim 1. Thus, Applicants submit that Claims 4-7, 13, 14, 17, 18, and 40 are patentably distinct over the cited reference at least for the reasons discussed above in conjunction with Claim 1.

Applicants submit that Claim 4 is further patentably distinct over Ishida, since the cited reference neither describes nor suggests "...*the current conductor portion further comprises a conductive clip directly and electrically coupled to the at least two of the plurality of leads*," as set forth in Claim 4. This arrangement is shown, for example, in FIG. 7. The Examiner uses element 2 (magnetic substance) of Ishida to teach a conductive clip, but element 2 is not directly coupled to leads 4 of Ishida.

Applicants submit that Claim 7 is further patentably distinct over Ishida, since the cited reference neither describes nor suggests "...*a thickness of the conductive clip is selected in accordance with a current passing through the conductive clip*," as set forth in Claim 7. Again, the Examiner uses element 2 (magnetic substance) of Ishida to teach a conductive clip. However, Applicants submit that no current flows through the magnetic substance 2 of Ishida.

Applicants submit that Claim 13 is further patentably distinct over Ishida, since the cited reference neither describes nor suggests "...*at least a part of the current conductor portion has a thinned rectangular cross section having a minimum dimension less than a thickness of other portions of said lead frame, the thinned rectangular cross section taken through a thickness direction of the current conductor portion, the thinned rectangular cross section resulting in an increased magnetic field proximate to the current conductor portion, and therefore, proximate to said one or more magnetic field transducers*," as set forth in Claim 13. The Examiner apparently uses element 1 (conductor) of Ishida to teach a lead frame having a thinned section 1a. For reasons described above in conjunction with Claim 1, Applicants submit that the conductor 1 of Ishida is not a lead frame at all.

Applicants submit that Claim 40 is further patentably distinct over Ishida, since the cited reference neither describes nor suggests "...*each one of the leads has a bend in a direction selected to result in each one of the leads being closer to the first surface of said substrate than to the second surface of said substrate throughout a length of the lead*," as set forth in Claim 40. This arrangement should be understood to be associated with the flip-chip arrangement recited in Claim 1. Namely, a flip-chip arrangement having bent leads will have the leads bent in the orientation claimed.

Applicants remind the Examiner that the first surface of the substrate is the surface upon which the one or more magnetic field transducers are disposed. The Examiner uses FIG. 5 of Ishida to teach the claimed arrangement of the substrate and lead frame. However, Applicants submit that Ishida does not teach a position of leads relative to a substrate at all. Furthermore, the leads shown in FIG. 5 of Ishida have no bend.

Applicants submit that independent Claim 29 is patentably distinct over Ishida, since the cited reference neither describes nor suggests "...*a lead frame having a plurality of leads and having a current conductor portion comprising a coupling of at least two of the plurality of leads, wherein the coupling of at least two of the plurality of leads comprises a loop, the at least two of the leads and the loop forming a continuous electrical path entirely formed of lead frame material*," as set forth in Claim 29. The Examiner uses element 1 (conductor) of Ishida to teach a lead frame with a loop. However, as described above in conjunction with Claim 1, Applicants again submit that the conductor 1 of Ishida is not a lead frame at all.

In view of the above, Applicants submit that Claim 29 is patentably distinct over Ishida.

Claims 30, 32, 33, and 41 depend from and thus include the limitations of Claim 29. Thus, Applicants submit that Claims 30, 32, 33, and 41 are patentably distinct over the cited reference at least for the reasons discussed above in conjunction with Claim 29.

For reasons described above in conjunction with Claims 1 and 13, Applicants submit that Claim 32 is further patentably distinct over Ishida, since the cited reference neither describes nor suggests "...*at least a part of the current conductor portion has a thinned rectangular cross section having a smallest dimension less than a thickness of other portions of said lead frame, the thinned rectangular cross section taken through a thickness direction of the current conductor portion, the thinned rectangular cross section resulting in an increased magnetic field proximate to the current conductor portion, and therefore, proximate to said one or more magnetic field transducers*," as set forth in Claim 32.

For reasons described above in conjunction with Claim 40, Applicants submit that Claim 33 is further patentably distinct over Ishida, since the cited reference neither describes nor suggests "...*each one of the leads has a bend in a direction selected to result in each one of the leads being closer to the first surface of said substrate than to the second surface of said substrate throughout a length of the lead*," as set forth in Claim 33.

For reasons described above in conjunction with Claim 1, Applicants submit that Claim 41 is further patentably distinct over Ishida, since the cited reference neither describes nor suggests "*said substrate and said lead frame are relatively disposed in a flip-chip arrangement resulting in the current conductor portion being proximate to said one or more magnetic field transducers, and further resulting in an increased sensitivity of the integrated circuit to a magnetic field*," as set forth in Claim 41.

In view of the above, Applicants submit that the rejection of Claims 1, 4-7, 13, 14, 17, 18, 29, 30, 32, 33, 40 and 41 under 35 U.S.C. §102(b) should be removed.

B. Dependent Claim 8 is not obvious over Ishida in view of Yangawa et al. (U.S. Patent Publication number 2001/0028115).

The Examiner rejects Claim 8 under 35 U.S.C. §103(a) as being unpatentable over Ishida in view of Yangawa et al. (U.S. Patent Publication number 2001/0028115).

Claim 8 depends from and thus includes the limitations of Claim 1. Thus, Applicants submit that Claim 8 is patentably distinct over the cited references at least for the reasons discussed above in conjunction with Claim 1.

In view of the above, Applicants submit that the rejection of Claim 8 under 35 U.S.C. §103(a) should be removed.

C. Dependent Claims 9, 36, and 37 are not obvious over Ishida in view of Williams (U.S. Patent Publication number 2005/0230843).

The Examiner rejects Claims 9, 36, and 37 under 35 U.S.C. §103(a) as being unpatentable over Ishida in view of Williams (U.S. Patent Publication number 2005/0230843).

Claims 9, 36, and 37 depend from and thus include the limitations of Claim 1. Thus, Applicants submit that Claims 9, 36, and 37 are patentably distinct over the cited references at least for the reasons discussed above in conjunction with Claim 1.

In view of the above, Applicants submit that the rejection of Claims 9, 36, and 37 under 35 U.S.C. §103(a) should be removed

D. Dependent Claims 10, 11, 15, 16, and 38 are not obvious over Ishida in view of Mayer et al. (U.S. Patent Publication number 2002/0179987).

The Examiner rejects Claims 10, 11, 15, 16, and 38 under 35 U.S.C. §103(a) as being unpatentable over Ishida in view of Meyer et al. (U.S. Patent Publication number 2002/0179987).

Claims 10, 11, 15, 16, and 38 depend from and thus include the limitations of Claim 1. Thus, Applicants submit that Claims 10, 11, 15, 16, and 38 are patentably distinct over the cited references at least for the reasons discussed above in conjunction with Claim 1.

Applicants submit that Claim 10 is further patentably distinct over Ishida, whether taken alone or in combination with Meyer et al., since the cited reference neither describes nor suggests "...*the current conductor portion has a current conductor portion axis and at least two of said one or more magnetic field transducers are disposed on opposite sides of the current conductor portion axis*," as set forth in Claim 10.

With regard to Claim 10, the Examiner asserts that "[i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to include two or more magnetic field [transducers] with the structure of Ishida for the purpose of detecting an angle of rotation." However, Applicants submit that it is not the mere inclusion of two magnetic field transducers that is set forth in Claim 10, but it is their placement relative to a current conductor portion axis. Neither Ishida nor Meyer et al. contemplate the claimed arrangement. Furthermore, the claimed arrangement is not intended to "detect an angle of rotation" as asserted by the Examiner, but instead to increase a sensitivity of the integrated circuit to a magnetic field generated by a current carried by the current conductor. For example, in conjunction with FIG. 5, which shows four magnetic field transducers, it is stated at page 12, lines 3-4, "...the current sensor 120 has four times the sensitivity of the current sensor 10 of FIG. 1."

In addition, as found in MPEP §2143.01, in order to establish a prima facie case of obviousness "...[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." (See e.g., In re Ratti, 270 F.2d 810, 123 USPQ 349 (C.C.P.A. 1959)).

The claimed magnetic field transducers are disposed on opposite sides of the current conductor portion axis. Referring to FIG. 5 of Ishida, Applicants submit that the modification to Ishida proposed by the Examiner would be very difficult or impossible to achieve in Ishida without entirely destroying the structure of Ishida. Therefore, one of ordinary skill in the art would not be motivated to provide this arrangement.

Applicants also make the Examiner aware that According to the Federal Register, Volume 72, No. 195, dated October 10, 2007, at page 57528, Part III of the section entitled "Examination Guidelines for Determining Obviousness under 35 U.S.C. 103 in View of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.*," an obviousness rejection may be made using the familiar teaching-suggestion-motivation (TSM) rationale... ." In Part III, it is also stated that "[a]lthough the Supreme Court in *KSR* cautioned against an overly rigid application of TSM, it also recognized that TSM is one of a number of valid rationales that could be used to determine obviousness." Thus, as one criteria used to establish prima facie obviousness, there should be some suggestion and motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.

Applicants submit that Claim 11 is further patentably distinct over Ishida, whether taken alone or in combination with Meyer et al., since the cited reference neither describes nor suggests "...*at least two of said one or more magnetic field transducers are rotated relative to each other for providing predetermined voltage output polarities*," as set forth in Claims 11. Applicants submit that Ishida and Meyer et al. do not teach or suggest relative rotations of magnetic field transducers, and thus, one of ordinary skill in the art considering these references would not motivated to do so.

Applicants submit that Claim 38 is further patentably distinct over Ishida, whether taken alone or in combination with Meyer et al., since the cited reference neither describes nor suggests "...*the current conductor portion has an edge bounding a surface of the current*

conductor portion, and wherein said one or more magnetic field transducers are disposed on the first surface of said substrate proximate to the current conductor portion and in a position such that neither the edge of the current conductor portion nor a surface of the current conductor portion overlaps said one or more magnetic field transducers," as set forth in Claim 38. Applicants submit that the claimed relative placement of the one or more magnetic field transducers and the current conductor portion is not taught or suggested by Ishida or Meyer et al, nor would one of ordinary skill in the art considering these references be motivated to provide such an arrangement. Applicants remind the examiner that the claimed current conductor portion is a part of the lead frame.

In view of the above, Applicants submit that the rejection of Claims 10, 11, 15, 16, and 38 under 35 U.S.C. §103(a) should be removed.

E. Dependent Claims 12 and 31 are allowable in their present dependent form.

The Examiner objects to Claims 12 and 31 as being dependent upon a rejected base claim, but indicates that Claims 12 and 31 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

For the above reasons, Applicants submit that independent Claim 1, from which Claim 12 depends, is patentably distinct over the cited references. Also for the above reasons, Applicants submit that independent Claim 29, from which Claim 31 depends, is patentably distinct over the cited references. Therefore, Applicants submit that Claims 12 and 31 are allowable in their present dependent form.

Conclusion

In view of the above, Applicants submit that the claims and the entire case are in condition for allowance and should be sent to issue and such action is respectfully requested.

The Assistant Commissioner is hereby authorized to charge payment of any additional fees associated with this communication or credit any overpayment to Deposit Account No. 500845, including but not limited to, any charges for extensions of time under 37 C.F.R. §1.136.

Respectfully submitted,

Dated: Nov 9, 2009

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Attachments:

(viii) Claims Appendix
(ix) Evidence Appendix
(x) Related Proceedings Appendix

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(viii) Claims Currently in the Application

1. (Previously Presented) An integrated circuit, comprising:

a lead frame having a plurality of leads and having a current conductor portion comprising a coupling of at least two of the plurality of leads, each one of the leads having a respective length;

a substrate having first and second opposing surfaces, the first surface proximate to the current conductor portion and the second surface distal from the current conductor portion, wherein at least some of the leads of said lead frame are electrically coupled to said substrate; and

one or more magnetic field transducers disposed on the first surface of said substrate, wherein said substrate and said lead frame are relatively disposed in a flip-chip arrangement resulting in the current conductor portion being proximate to said one or more magnetic field transducers, and further resulting in an increased sensitivity of the integrated circuit to a magnetic field.

2. (Cancelled)

3. (Cancelled)

4. (Previously Presented) The integrated circuit of Claim 1, wherein the current conductor portion further comprises a conductive clip directly and electrically coupled to the at least two of the plurality of leads.

5. (Original) The integrated circuit of Claim 4, wherein said substrate is disposed having the first surface of said substrate above said conductive clip and the second surface of said substrate above the first surface.

6. (Original) The integrated circuit of Claim 4, wherein said substrate is disposed having the first surface of said substrate below said conductive clip and the second surface below the first surface.

7. (Original) The integrated circuit of Claim 4, wherein a thickness of the conductive clip is selected in accordance with a current passing through the conductive clip.

8. (Original) The integrated circuit of Claim 1, wherein said substrate has at least one bonding pad coupled to a corresponding one of the plurality of leads with a bond wire.

9. (Previously Presented) The integrated circuit of Claim 1, wherein said substrate is coupled to said lead frame with a selected one of a solder ball, a gold bump, a eutectic and high lead solder bump, a no-lead solder bump, a gold stud bump, a polymeric conductive bump, or an anisotropic conductive paste coupled to a corresponding one of the plurality of leads.

10. (Original) The integrated circuit of Claim 1, wherein the current conductor portion has a current conductor portion axis and at least two of said one or more magnetic field transducers are disposed on opposite sides of the current conductor portion axis.

11. (Original) The integrated circuit of Claim 1, wherein at least two of said one or more magnetic field transducers are rotated relative to each other for providing predetermined voltage output polarities.

12. (Previously Presented) The integrated circuit of Claim 1, wherein at least a part of the current conductor portion has a T-shaped cross section, the T-shaped cross section taken through a thickness direction of the current conductor portion, the T-shaped cross section resulting in an increased magnetic field proximate to the current conductor portion, and therefore, proximate to said one or more magnetic field transducers.

13. (Previously Presented) The integrated circuit of Claim 1, wherein at least a part of the current conductor portion has a thinned rectangular cross section having a minimum dimension less than a thickness of other portions of said lead frame, the thinned rectangular cross section taken through a thickness direction of the current conductor portion, the thinned rectangular cross section resulting in an increased magnetic field proximate to the current conductor portion, and therefore, proximate to said one or more magnetic field transducers.

14. (Original) The integrated circuit of Claim 1, further comprising at least one amplifier disposed on said substrate.

15. (Original) The integrated circuit of Claim 14, wherein the at least one amplifier provides an output signal proportional to a sum of signals generated by at least two of said one or more magnetic field transducers.

16. (Original) The integrated circuit of Claim 14, wherein the at least one amplifier forms a summing arrangement coupled to four of said one or more magnetic field transducers.

17. (Original) The integrated circuit of Claim 1, further comprising a flux concentrator disposed proximate said one or more magnetic field transducers.

18. (Original) The integrated circuit of Claim 1, further comprising a flux concentrating layer disposed proximate the second surface of said substrate.

19-24. (Canceled)

25-28. (Canceled)

29. (Previously Presented) An integrated circuit, comprising:

a lead frame having a plurality of leads and having a current conductor portion comprising a coupling of at least two of the plurality of leads, wherein the coupling of at least

two of the plurality of leads comprises a loop, the at least two of the leads and the loop forming a continuous electrical path entirely formed of lead frame material;

a substrate having first and second opposing surfaces, the first surface proximate to the current conductor portion and the second surface distal from the current conductor portion, wherein at least some of the leads of said lead frame are electrically coupled to said substrate; and

one or more magnetic field transducers disposed on the first surface of said substrate and proximate to the loop such that the one or more magnetic field transducers are responsive to a current flowing through the loop.

30. (Previously Presented) The integrated circuit of Claim 29, wherein at least one of the one or more magnetic field transducers is disposed within an inner dimension of the loop.

31. (Previously Presented) The integrated circuit of Claim 29, wherein at least a part of the current conductor portion has a generally T-shaped cross section, the cross section taken through a thickness direction of the current conductor portion, the T-shaped cross section resulting in an increased magnetic field proximate to the current conductor portion, and therefore, proximate to said one or more magnetic field transducers.

32. (Previously Presented) The integrated circuit of Claim 29, wherein at least a part of the current conductor portion has a thinned rectangular cross section having a smallest dimension less than a thickness of other portions of said lead frame, the thinned rectangular cross section taken through a thickness direction of the current conductor portion, the thinned rectangular cross section resulting in an increased magnetic field proximate to the current conductor portion, and therefore, proximate to said one or more magnetic field transducers.

33. (Previously Presented) The integrated circuit of Claim 29, wherein each one of the leads has a bend in a direction selected to result in each one of the leads being closer to the first surface of said substrate than to the second surface of said substrate throughout a length of the lead.

34-35. (Canceled)

36. (Previously Presented) The integrated circuit of Claim 1, further including a solder ball disposed to electrically couple said substrate to said lead frame.

37. (Previously Presented) The integrated circuit of Claim 1, further including a stud bump disposed to electrically couple said substrate to said lead frame.

38. (Previously Presented) The integrated circuit of Claim 1, wherein the current conductor portion has an edge bounding a surface of the current conductor portion, and wherein said one or more magnetic field transducers are disposed on the first surface of said substrate proximate to the current conductor portion and in a position such that neither the edge of the current conductor portion nor a surface of the current conductor portion overlaps said one or more magnetic field transducers.

39. (Canceled)

40. (Previously Presented) The integrated circuit of Claim 1, wherein each one of the leads has a bend in a direction selected to result in each one of the leads being closer to the first surface of said substrate than to the second surface of said substrate throughout the length of the lead.

41. (Previously Presented) The integrated circuit of Claim 29, wherein said substrate and said lead frame are relatively disposed in a flip-chip arrangement resulting in the current conductor portion being proximate to said one or more magnetic field transducers, and further resulting in an increased sensitivity of the integrated circuit to a magnetic field.

(ix) Evidence

None

(x) Related Proceedings

None